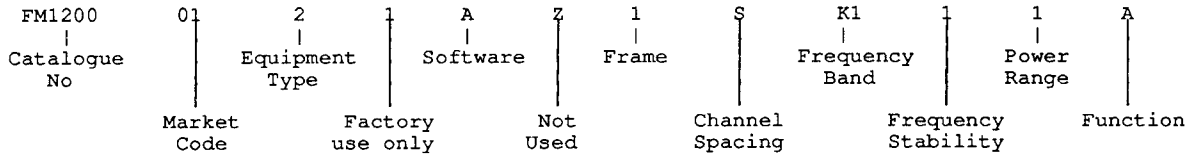
EQUIPMENT VARIATIONS

The sub-assemblies fitted to the transceiver will vary according to the role in which it is used. The complement of sub-assemblies for any particular equipment is indicated by an ordering code number marked on the equipment caseback. A typical order code number is given below, together with a list of codes which are not self-explanatory.



Market Code

01 Standard production
02 France
03 West Germany
09 Canada
12 Finland
19 Malaysia
30 Hong Kong

Equipment Type

2 FFSK Transceiver Type FM1200
3 FFSK Transceiver Type FM1300

Software

0 Less EEPROM and EPROM
A FM1200, Standard Console
B FM1200, Keypad Console
C FM1300, Standard Console
D FM1300, Keypad Console

Frame

1 Standard Frame
2 Extended Frame (required for Keypad Console and/or External MODEM)

Channel Spacing

S 12,5kHz
R 20kHz
V 25kHz

Frequency Band

E0 68 - 88MHz
B0 132 - 156MHz
A9 146 - 174MHz

K1 174 - 208MHz
K2 192 - 225MHz

TM 400 - 440MHz
T4 425 - 450MHz
U0 440 - 470MHz
W1 470 - 500MHz
W4 500 - 520MHz

Frequency Stability

1 ±5ppm
2 ±2ppm

Power Range

1 Standard VHF (1-25/30W)
2 Standard UHF (6-25W)
3 Low Power UHF (1-6W)

Function

0 Less Control/Digital-Signalling PWB
A FM1200 (FM)
B FM1200 with Modem Interface (FM)
C FM1300 (FM)
D FM1300 with Modem Interface (FM)
E FM1200 (PM)
F FM1200 with MODEM Interface (PM)
G FM1300 (PM)
H FM1300 with MODEM Interface (PM)

SECTION 3
TECHNICAL DESCRIPTION

CIRCUIT SUMMARY

The transceiver consists of five PWB assemblies as in FM1100, but the Control PWB is replaced by the following assembly:-

DIGITAL SIGNALLING	comprising Non-Prescribed Data PWB (optional), main transceiver microprocessor with clock oscillator, EPROM, EEPROM, RAM, Shift Registers, timers, 30V generator and FFSK signalling circuits comprising microprocessor, EPROM, Address Latch, RAM, MODEM and peripheral devices.

All FM1200 control and signalling functions are provided by the Control/Digital Signalling PWB assembly. This PWB contains two 80C31 microprocessors IC312,IC548. IC312 acts as the main control for the FM1200, and communicates with peripheral devices (eg consoles and data programmers) via a serial bus. The bus is interrogated on a regular basis and the state of the FM1200 altered depending on information received. Control of the analogue part of the radio is achieved via serially driven shift registers, the outputs of which directly control the analogue functions. Certain internal voltages within the FM1200 radio are monitored via an Analogue-to-Digital (A-to-D) converter (IC301) and an input shift register (IC303). Customisation data, such as the frequency band and the key and indicator functions, are held in EEPROM (IC311) to which the microprocessor has access. IC548 controls all 'over the air' signalling via an FFSK MODEM (IC546). It decodes the incoming bit stream from the MODEM to detect valid signalling. Relevant signalling messages are then passed via a dedicated serial bus to the control microprocessor (IC312). Encoding of FFSK for transmission is performed by the signalling microprocessor which outputs binary data to the MODEM which converts it into FFSK audio.

The Non-Prescribed Data PWB allows interface between the radio and an externally-mounted MODEM. Sequential tone information generated by the signalling microprocessor may be processed on this PWB prior to transmission by the radio.

CONTROL/DIGITAL SIGNALLING PWB

Power Supply Circuits

When the FM1200 radio is switched on, unregulated DC is supplied to the Control PWB from the Analogue PWB via SKTB. This is used to supply two single chip voltage regulators which provide outputs of 5V and 8V respectively. The 5V line is used to feed the logic control circuitry and 8V is used to supply the audio circuitry for the FFSK signalling.

The unregulated DC input is also used to supply the 30V generator circuit which is required for the synthesiser loop filter. This is generated by IC318, a charge pump device. Adjustment of the 30V output is achieved by RV301 which senses the rectified and smoothed output of the device and feeds it back to its control pin.

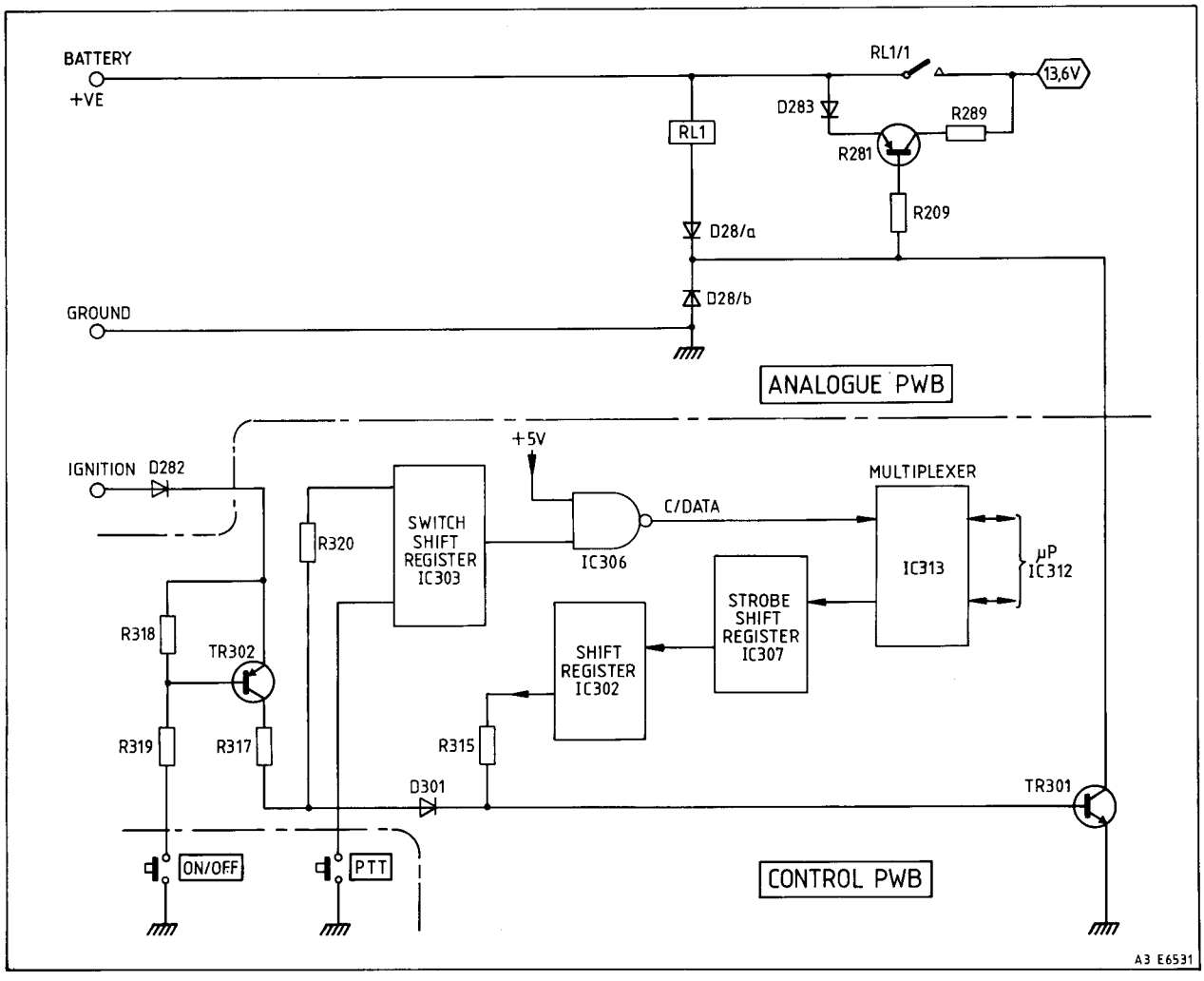


Fig 3.1 Power Supply Circuits Block Diagram

ON/OFF CIRCUIT

DC power from the vehicle battery (or other external PSU) is switched on or off by a relay mounted on the Analogue PWB. To switch the equipment on, the Ignition line must be connected to the external DC supply and the incoming on/off control line grounded (eg: by pressing the console on/off switch or plugging in a data programmer). TR302 effectively forms an AND gate with the ignition and on/off inputs. When the ignition line (TR302 emitter) is high and on/off line (TR302 base resistor) is low, TR302 switches on. This in turn switches on TR301, the collector load of which is the power on/off relay. When this occurs, the control microprocessor can hold the FM1200 radio on by setting Q4 of IC302 high. This feature also enables the data to be saved to EEPROM after detecting switch off. The state of the on/off line is monitored via the D0 input of the switch input register IC303.

CONTROL MICROPROCESSOR

The control processor uses a nominal 12MHz clock frequency. This is provided by TR307, TR306, TR305 and XL301 which form a pullable oscillator circuit. On power up the microprocessor requires to be reset. This is performed by IC314 which applies a positive pulse of approx 20ms at the reset input of the microprocessor when it detects the 5V supply rail ramping up. In normal operation no further reset pulses should be applied.

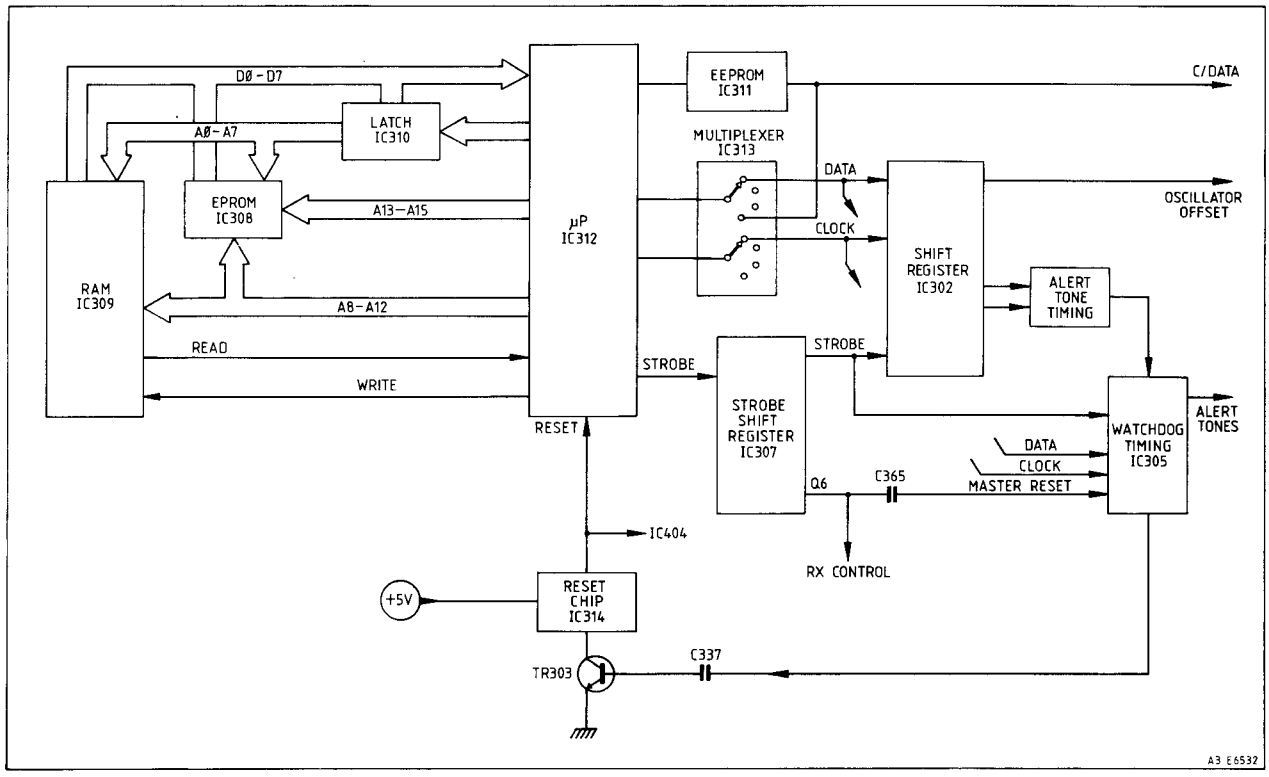


Fig 3.2 Microprocessor Block Diagram

The microprocessor executes software code held in a 64K EPROM (IC308) which it accesses via its external address/data bus D0 to D7 and A8 to A15. The device operates on a 8-bit wide data bus and 16-bit address bus. In order to reduce the pin count of the 80C31, the low order address bus is multiplexed with the data bus. To separate these functions an address latch (IC310) is used. This acts as a transparent latch gated by its LE input. When the microprocessor outputs its low order address it also sends out a positive pulse on its ALE line which gates the low address through to the output of the latch. Also connected to the external bus is an 8k x 8 static RAM (IC309) which also uses the address latch, but control of Read and Write functions is via two separate control lines from the microprocessor, "/RD" and "/WR".

To avoid data corruption during short power interruptions (FM1200 only), the RAM supply voltage is fed via a series diode and reservoir capacitor, which can maintain the contents of the RAM for at least 20 seconds. To avoid corruption at reset the reset pulse is inverted by TR309 which sets CHIP SELECT 'low', disabling the RAM for the duration of the reset pulse.

When first switched on, the microprocessor software will initialize the FM1200 radio by commands sent on the serial bus. Ports 3.1 and 3.0 on IC312 connect to a serial UART held on chip. This can be configured in a number of different ways determined by the radio software. The FM1200 utilizes two of the available UART modes and further sub-divides these depending on whether the bus connects to an external device or devices internal to the radio. A bi-directional multiplexer IC312 is used to connect the serial UART to each bus in turn. Selection is controlled by P1.1 and P1.0 of the microprocessor. The operation of each bus is explained below:

INTERNAL EXPANSION BUS (IEB)

This bus is formed by lines CLK and C/DATA from pins 11 and 4 of the multiplexer IC313. It is used to drive a number of Input and Output shift registers contained on both the Control PWB and the Analogue PWB.

To write to an output shift register (74HC4094), the microprocessor writes data into the shift registers on the C/DATA line. The Clock signal is provided by the CLK line which is connected to all shift registers on this bus. To write to any of the shift registers, it first sends out an 8-bit data byte corresponding to the output pattern it wishes to write to the selected shift register. This data will be stored in the strobe shift register (IC307). This is immediately followed by an address byte for the selected shift register. As the address byte is clocked into the strobe shift register the previous data byte is clocked out of it (on pin 10) and is clocked via the data inputs into all the output shift registers on the bus. By applying a pulse on P1.4, the strobe and output enable of IC307 are momentarily enabled causing, the address byte to appear on its parallel outputs. This byte will be chosen so that a '1' is passed to the strobe of the required output register, hence only that shift register will be strobed, latching the required data byte onto its parallel outputs.

To read from the switch input shift register (74HC165), a similar technique is used. Bit Q4 of the strobe shift register is sent momentarily low. This is connected to the shift load input of the Switch Input Register IC303, causing data on its parallel inputs to be loaded into IC303's internal shift register. By applying eight clock pulses on the CLK line the data is serially clocked out from IC303 pin 9 via an open collector NAND gate (IC306) and read in by the microprocessor. To avoid contention when writing to the C/DATA line from the microprocessor, the open collector output of this NAND gate must be set high. This is achieved by sending eight clock pulses to the switch input register (which has its serial input tied to 0V), thus filling the shift register with '0's.

The switch input register is read every 10ms. Output devices on this bus are written to as required.

EXTERNAL EXPANSION BUS (EEB)

This bus operates in an identical manner to the Internal Expansion Bus but uses separate CLK, C/DATA and Strobe lines. It is used to interface with certain ancillaries such as the Keypad Microphone which has internal shift registers in it. Each ancillary also contains a separate strobe shift register which is enabled by a strobe signal from P1.2 of the microprocessor. IC315 is used as a line driver. When writing out on the bus the microprocessor enables this line driver by switching P1.3 low. Taking P1.3 low also sets the output of a NAND gate in IC306 high during writing to avoid bus contention. When P1.3 is set high the microprocessor reads from the bus. Incoming data is buffered by IC315 and passed via IC306 (now enabled) and IC313 to microprocessor IC312.

When first switched on, the microprocessor will read the bus to detect if any ancillary is connected. If so, it will 'poll' the bus every 10ms; otherwise the bus will be ignored until the FM1200 radio is next switched on or is reset.

EXTERNAL MESSAGE BUS (EMB)

In this mode the UART is set up as a 378 kilobit serial link communicating on the TxD and RxD lines on SKTC/PLA. The EMB is used to communicate with complex peripherals such as the Standard Console or the Portable Data Programmer. At switch-on, IC312 sends out a series of pre-defined messages to all the possible peripherals which can be connected to the radio. If connected, the peripheral will respond to the message and IC312 will then send out messages to the device every 10ms. If a peripheral device is not connected at the time of switch on, and hence doesn't reply, IC312 will assume that it is not connected and send no more messages to that device.

INTERNAL MESSAGE BUS (IMB)

This bus is similar to the EMB. However, the signalling microprocessor is the only device connected to it. To ensure fast communication from the signalling microprocessor to the control microprocessor, use is made of the control micro's INT0 input (to avoid having to wait for the control micro to request the transaction).

Analogue-to-Digital (A-to-D) Converter

IC301 is an 8-bit resolution A-to-D converter. It is used for monitoring the state of various voltages from the RF and audio parts of the radio. The following inputs are used:

1 Tune Volts:	This is used for monitoring the VCO tuning voltage. If it is outside a certain range, it will increment a hardware error count in EEPROM. The radio will, however, remain operational.
2 Supply voltage:	This is used when monitoring transmitter power to detect whether a reduction in transmitter power was caused by a reduced supply voltage.
3 Tx Temp:	This is connected to a thermistor circuit held in the transceiver casting. If an excessive temperature is detected, the control unit will reduce the transmitter power by steps until the temperature falls again, or zero power is reached. If zero power is reached, the FM1200 radio will switch back to receive mode.
4 Noise Level:	This is used to determine the quieting of the receiver and, if appropriate, open the squelch.
5 RSSI:	This is a DC signal from the IF amplifier, used to determine the signal strength. It is used for squelch control and when hunting for a suitable channel to communicate with the trunked radio network.
6 Power Level:	This input is from a diode detector circuit on the PA. It is used to monitor the transmit power. If excessive or too little power is detected, the output power is reduced in steps in the same way as with excessive temperature.
7 Volume:	This input comes from the console volume potentiometer which gives a DC level depending on its setting. The microprocessor sets the digital audio attenuator on the analogue board according to this value.
8 Hook/Facility Switch:	This is an input from the microphone. These switches are connected with resistors in such a way that the voltage on this pin depends on which combination of switches are closed, and enables their operation to be detected by the microprocessor software.

The A-to-D convertor uses the 5V rail on the Control PWB as a reference. It is driven from the Internal Expansion Bus using a method similar to that employed for the input and output shift registers. To enable a conversion, the microprocessor uses the IEB to inform the device which of the inputs is required to be converted. It then takes P3.5 low to signal that conversion should now take place. The chip uses the ALE line from the microprocessor as its system clock. (On average ALE will run at 2MHz as code is executed from the EPROM.)

Alert Tone Generator/Watchdog Timer

The alert tone generator is a simple RC inverter oscillator made up of C326,R328 to R331 and IC305 which contains on-chip inverters. The alert tone frequency and gating is controlled by IC302. The shift register outputs of IC302 are used to modify the oscillator's RC time constant depending on which alert tone is required, and the Q7 output is used to gate these tones on or off. The resultant audio is mixed with the loudspeaker audio on the Analogue PWB. IC305 also contains a series of cascaded dividers which reduce the RC oscillator frequency down by factors of 2. If allowed to run for long enough, a pulse will appear on the divider output at pin 1, causing TR303 to switch on and the reset chip to send a pulse to reset the microprocessors. In practice, this is prevented by C365, which transmits pulses from the strobe shift register and resets the cascaded dividers within IC305. However, if the software is not running properly, this will not occur, and a reset pulse will be generated.

Microprocessor Oscillator

IC312 is supplied directly from the oscillator output and supplies the signalling microprocessor via an internal buffer from its XTAL2 output. XL301, TR305 and associated components form a standard Colpitts oscillator. Transistors TR306, TR307 are used to switch in a different crystal load capacitance depending on the logic level at Q1 of IC302. The oscillator frequency can thus be offset slightly when a direct harmonic of the crystal falls close to the current receive frequency. Each time the radio tunes to a new channel, the microprocessor calculates whether frequency offset is necessary, or not. When transmitting, the oscillator is always set to its nominal 12,096MHz.

EEPROM

IC311 is a serial EEPROM used for storage of all customisation data. Depending on customer requirements a 512 byte or 2 kilobyte device is fitted (X2404 and X24C16 respectively). Electrical operation with each device is similar. On power up, the FM1200 radio reads customisation data into RAM before normal operation is commenced. The device uses I^2C protocol which utilizes a CLK and DATA line to communicate with the microprocessor. When the microprocessor is communicating with this device, it uses the C/DATA line on the IEB to send and receive data, but generates a separate clock output from P1.5.

If any customisation data is modified (eg by a PDP), the microprocessor will save the changes to EEPROM at switch-off. If there are a substantial number of changes to the customisation data, there will be a noticeable delay between switching off at the console and the FM1200 internal relay opening (power down).

External Alert

This circuitry can be used as either an input or an output. In normal operation this is used as an output to switch an external device (eg a car horn) when the mobile is called. In this case, the microprocessor sets p1.6 high to switch on darlington pair TR308/TR304. The Darlington pair connect to the External Alert pin on the external power socket. This output is also sensed by the microprocessor via R324 and the switch input register. At switch-on, P1.6 is set low and hence TR304 collector floats high. If the External Alert pin is taken to 0V before switch-on, the microprocessor detects that it is being used as an input. This mechanism is used to place the FM1200 radio into test mode (see Section 4 of TP253).

FFSK Encoder/Decoder

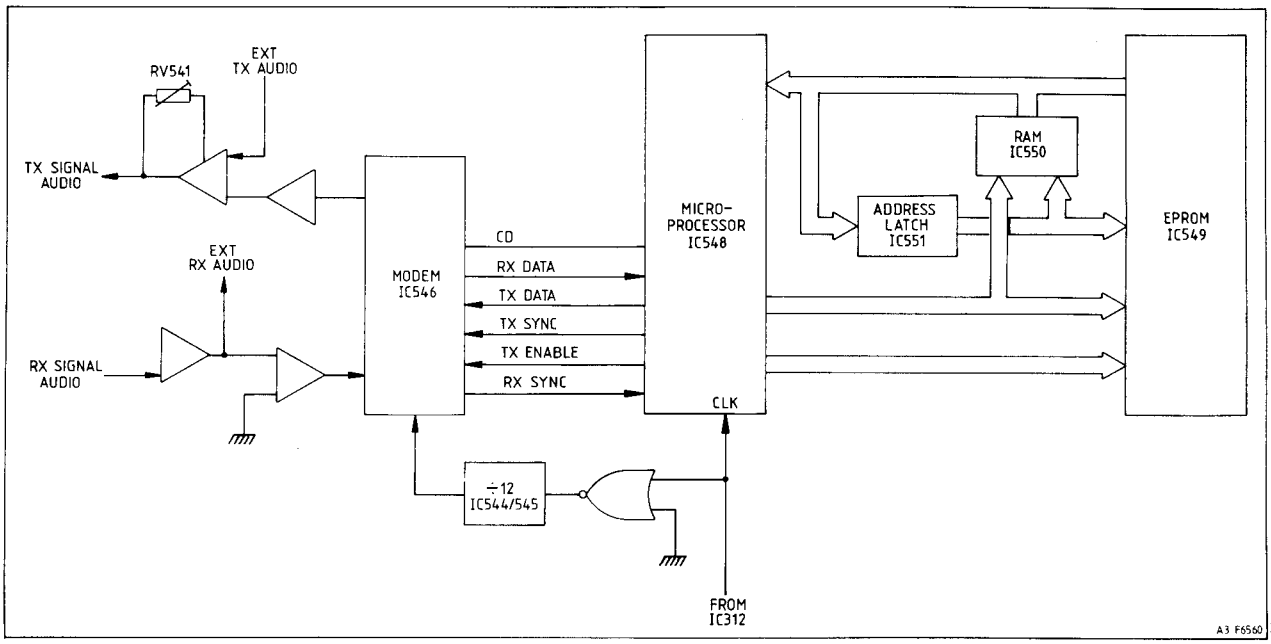


Fig 3.3 Digital Signalling Block Diagram

FFSK functions are controlled by microprocessor IC548 which relies on master processor IC312 for its clock signal (defining processing speed) and instructions from the console. Signalling data is stored in EPROM IC549, which is accessed via 8-bit address latch IC551. Data from the EPROM is loaded into RAM IC550 at switch on.

MODEM IC546 is a full duplex device, ie it can decode while encoding. Tx Data is clocked out from IC546 by pulses on the Tx Synch line from microprocessor IC548. Similarly, Rx Data is clocked in by Rx Synch pulses from IC548. A 1,008MHz clock signal is required to drive IC548; this is derived from IC312 clock. As IC312 clock runs at 12,096MHz, it is applied to flip-flops IC544, IC545, which divide the signal by 12 to produce 1,008MHz.

Signalling Microprocessor

The signalling microprocessor is also an 80C31 device and has external RAM (IC550) and EPROM (IC549) operating in a similar fashion to the main transceiver microprocessor. The signalling microprocessor interfaces with the FFSK MODEM IC546 via a number of control lines. The MODEM itself is a duplex device which is configured so that its receiver is permanently enabled. The transmit section generates 1800Hz and 1200Hz tones from incoming Tx Data sent to it at a bit rate of 1200bps. Tones and bit rate are generated by the MODEM from a reference frequency of 1,008MHz at its XTAL1 input. This is derived from the 12,096MHz microprocessor oscillator and divided by 12 by J-K flip-flops IC544 and IC545.

MODEM

CD - CARRIER DETECT

Carrier Detect is a logic signal sent from the MODEM receiver to the signalling microprocessor. A series of filters within the MODEM are set up to detect FFSK signalling frequencies. When FFSK signals are detected, the CD line goes 'high'. Operational speed of the CD line is determined by the value of C558 (connected to the CDT MODEM input) which controls a time constant within the IC.

RX DATA

This is the received serial data stream from the FFSK MODEM, which is read by the signalling microprocessor.

RX SYNC

This is a 1200Hz square-wave output from the MODEM, which is synchronised to the RxDATA output and is used to generate an interrupt to the microprocessor when the next bit of valid data is present on RxDATA. When no signalling or a noisy signalling is received, this output will exhibit 'jitter' as it repeatedly resynchronises.

TX EN - (TX ENABLE)

When the microprocessor wishes to transmit a message, it takes this line 'low' to enable the FFSK transmitter.

TX SYNC

This output is a 1200Hz square-wave from the MODEM. It is used to interrupt the signalling microprocessor to signal that it should output the next bit of data to be encoded. It will only be active when the TxEN is 'low'.

TX DATA

This line is used by the signalling microprocessor to output the data stream to be converted by the MODEM to FFSK audio.

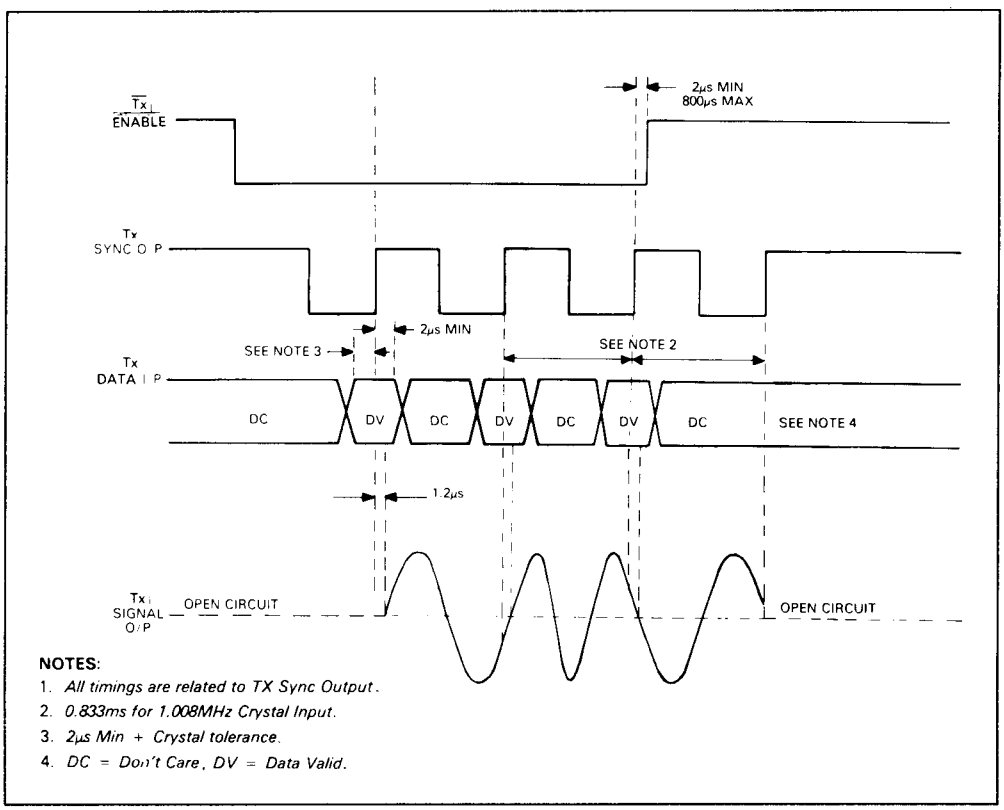


Fig 3.4 FFSK Transmit Timing Diagram

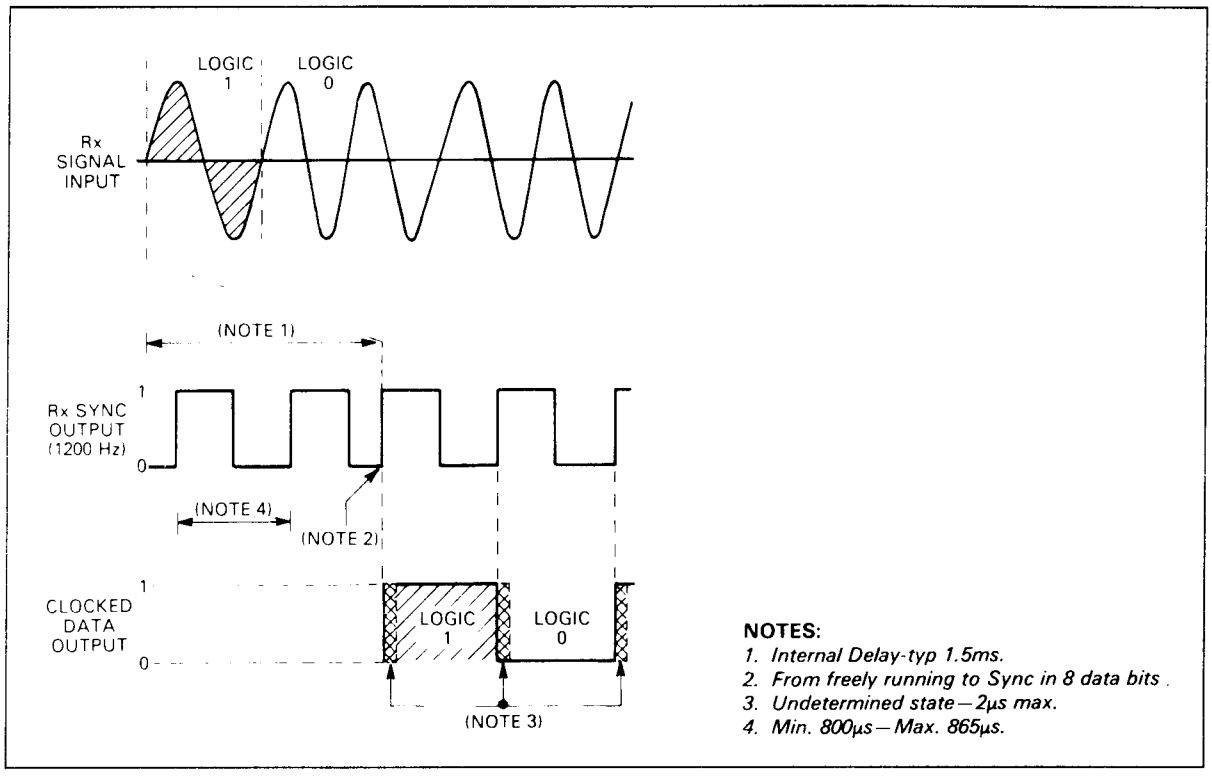


Fig 3.5 FFSK Receive Timing Diagram

FFSK Analogue Circuitry

FFSK is outputted from the Tx Audio output of IC546 when outgoing signalling is in progress. This signal is taken to inverting operational amplifier IC543, the gain of which is set via RV541 and associated resistors. The gain of this stage is altered to control the AF level to the FM modulator and hence set the required frequency deviation for data signalling. The bias pin from the MODEM is used to create a half rail for the operational amplifiers and is buffered by a unity gain amplifier (IC541). This output is fed through a low pass filter with a break point of approximately 15kHz to remove any high frequency components from the waveform. It is then fed to the modulator on the Analogue PWB.

Unfiltered receiver audio is fed (without filtering) from the Analogue PWB. It is buffered by part of IC541 and fed to a clipper amplifier (IC541) which uses a pair of back-to-back diodes and feedback network to supply the correct level of clipped audio signal to the MODEM. It is then buffered and presented to the MODEM via a unity gain operational amplifier. A separate half rail is provided for the receive circuit by R544, R545 and C546.

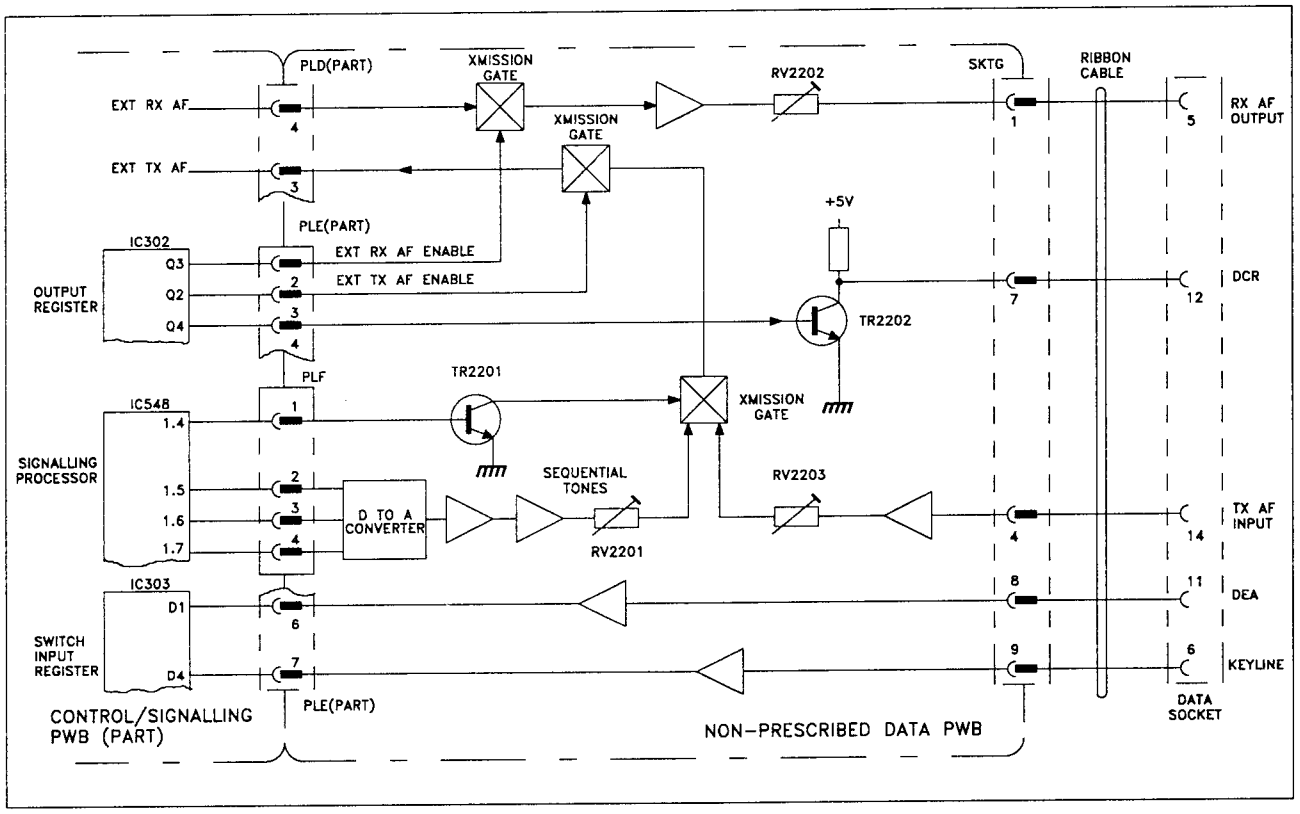


Fig 3.6 Non-Prescribed Data PWB Block Diagram

MODEM Interface

Unfiltered receiver audio at PLD4 is gated by IC204 which is enabled by the External Audio enable input, and then amplified by buffer IC205 to a 600ohm output on the front panel data socket. The gain of this section is adjusted by RV2202. Transmit audio from the external MODEM is applied via SKTG4 to IC2205 and is gain adjusted by RV2203. It passes two switches, the first, controlled by the signalling processor (Port 1.4), switches between external MODEM input and the on-board sequential tone encoder. This switch is set by default to enable transmission of data from the external MODEM, execpt when sequential tones are being generated. The second switch mutes audio to the Control PWB and is controlled by the Tx Audio Enable line. This switch is open except when accepting external MODEM data or sequential encode tones are generated. Transmitter audio is fed, via the Control PWB, directly into the modulation circuits of the Analogue PWB without any filtering.

The Tx and Rx Audio enable lines operate at +5V logic levels whereas the switches require +8V logic levels. Level shift for each audio enable line, DEA and KEYLINE is provided by a section of IC2201. IC2201 is a Schmitt Trigger buffer. Hysteresis is provided via C2238, R2254, R2253, R2255.

DEA — Data Equipment Available - informs radio that external device is ready to accept data.

KEYLINE — An external PTT operated from within the External MODEM. Both KEYLINE and DEA are read on separate lines of the Control PWB Switch Input Register, and will only key the transmitter when a data call is in progress.

DCR — Data Channel Ready - signal to external device inviting data to be sent. DCR will not be in 'ready' state until the radio is transmitting. This line is buffered by TR2202.

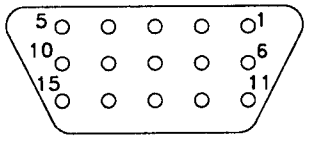
A +13V power source derived from the radio power supply is available for powering an external device. This supply is protected by a 250mA fuse.

Sequential Tone Encoding

Sequential signalling is controlled by the signalling microprocessor on the Control PWB. Encode tones are generated by the microprocessor on port 1 (pins 7, 8, 9), as a series of square-waves which are summed together by Digital-to-Analogue Converter (DAC) IC2202 and IC2203. The product is a 5-stepped squared waveform which is filtered by another stage of IC2203 to produce an acceptable sinusoidal waveform. The signal then passes via preset level potentiometer RV2201 (TONE DEVIATION LEVEL) before gating to the external Tx audio line.

Connections external to the radio are made by SKTG, which connects to a 15-way data socket (similar to the microphone connector). The pin numbering of the socket is as follows:

Pin Number	Connection
5	Rx Audio live
10	Rx Audio ground (analogue)
1	+13,6V
14	Tx Audio live
9	Tx Audio ground (analogue)
12	DCR (Data Channel Ready)
6	Keyline live
7	Keyline ground (digital)
11	DEA live
8	DEA ground (digital)



(VIEWED FROM FRONT)

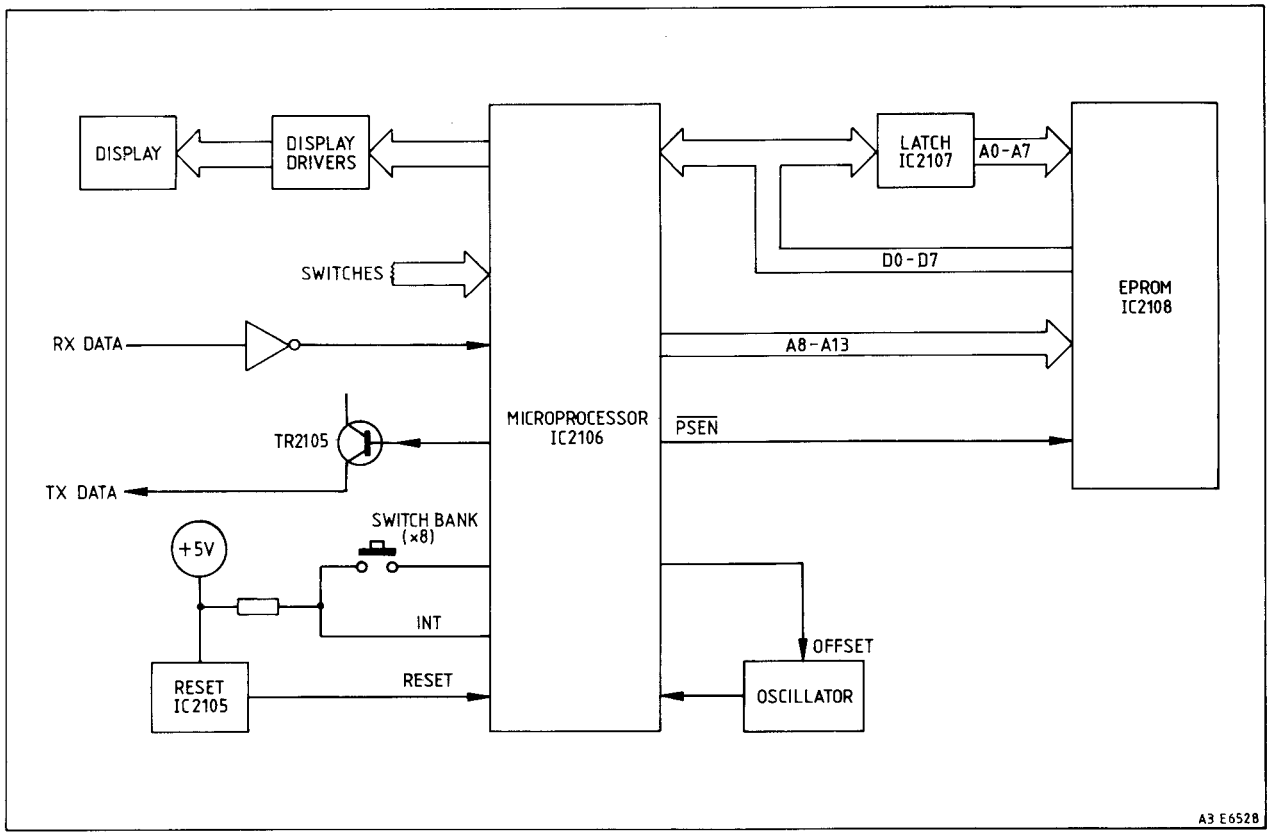


Fig 3.7 Standard Console Block Diagram

Microprocessor IC2106 receives and issues control information to and from peripheral devices. System operation is defined by a set of instructions either stored in EPROM IC2108 or masked within the processor, depending on the presence of R2103 or R2102. When R2103 is fitted, instructions are masked within the processor and IC2107 and IC2108 may be omitted from the PWB. When R2102 is fitted, instructions are read from EPROM IC2108.

Instructions within EPROM IC2108 are read by the microprocessor by first addressing the EPROM via the 8-bit latch IC2107 and then taking PSEN 'low'. Instructions are read and processed at a speed defined by the microprocessor crystal oscillator frequency and on-board oscillator-dividers. The microprocessor cycles through a loop until an 'interrupt' signal is received.

The microprocessor is reset at pin 10 by Reset chip IC2105 whenever the +5V regulated line drops below an acceptable level. The Console PWB has its own +5V regulator IC2104, which receives power from the transceiver 13,6V line at PLA1.

Two interrupt inputs to the microprocessor, INT0 and INT1, are held at +5V by R2105 and R2104 respectively. When a display button key is depressed, a 'low' is applied to the relevant input to inform the microprocessor to look for key switch action. Switches SW2102-SW2105 put an interrupt on IC2106 pin 14 (INT0) and switches SW2106-SW2109 put an interrupt on IC2106 pin 15 (INT1).

The microprocessor receives data from the transceiver which informs it as to whether clock offset is required for the current channel or not. If offset is required, the microprocessor puts a 'low' on TR2103 base via bridge R2116/R2115. This switches off TR2103 which in turn switches on TR2102, effectively putting C2117 in parallel with C2116 and pulling XL2117 down onto its calibration frequency. The frequency offset is not sufficient to disrupt the operation or timing of the microprocessor (see 'Control PWB').

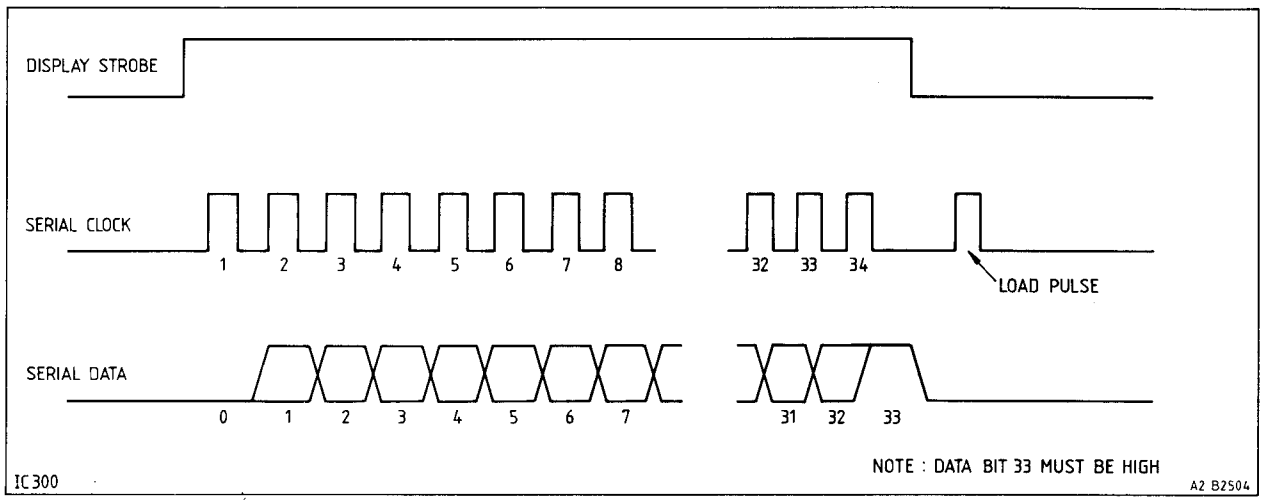


Fig 3.8 Display Driver Timing Diagram

For correct operation, LCD2101 requires a square-wave of approximately 50Hz which is applied to the LCD common backplane, with individual display segments driven in phase to switch them off, or out of phase to switch them on.

Two display drivers IC2101 and IC2102 are employed: these have a three line serial bus structure enabling serial data transfer from IC2106. Both have on-board oscillators; only that in IC2102 is used to drive the LCD backplane, the oscillator in IC2101 is disabled by grounding pin 3.

When the microprocessor makes the DISPLAY STROBE line high, data from the microprocessor is clocked into the driver by SERIAL CLOCK pulses, also provided by the microprocessor. Data is locked into the driver when the DISPLAY STROBE is low. At the 35th clock pulse the data is transferred to the LCD; LCD segments are switched on as a result of corresponding 'high' serial data bits. As data is locked into the driver, the display is updated only when display information needs to be changed, ie as a result of pressing a console button.

The display backlight is switched on and off by the microprocessor via IC2103a,b,c, and TR2104.

TEST MODE

To align the radio, it is neccessary to override its signalling protocol. This is achieved by setting it into test mode.

To select test mode, switch off the radio and then connect pin 6 of the Battery Lead Assembly to pin 4 (0V).

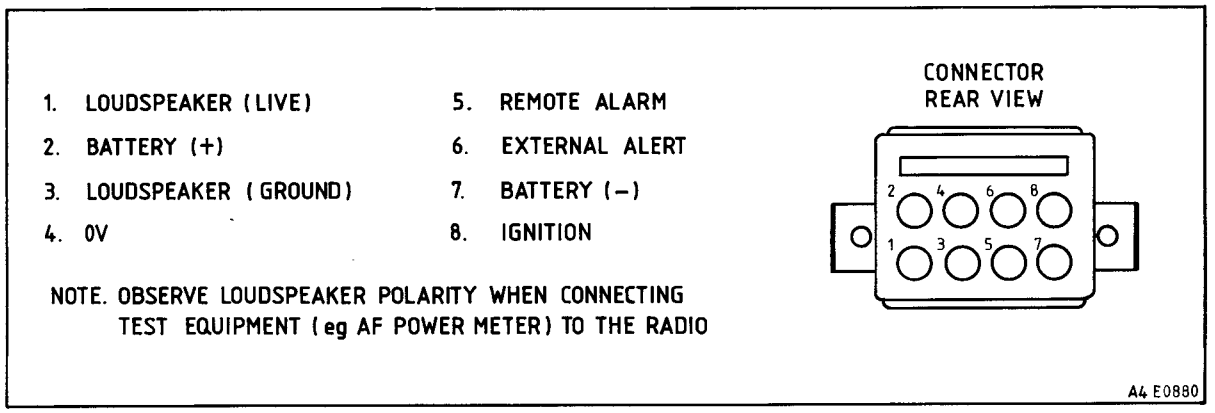


Fig 4.2 Battery Lead Connector

On selection of test mode, FM1200 radios tune to the Base Channel (Channel 0). In order to fully align the radio it will be necessary to select channels at the lower, middle and upper ends of the frequency band of the radio. The radio calculates its receiver and transmitter channels from a synthesiser base code. In order to select other frequencies this code must be changed. Note that it is only possible to select alignment channels in Test Mode.

Table 4.1 - Synthesiser Codes for Test Frequencies (FM1200 only)

Freq (MHz)	Code	Freq (MHz)	Code
68	10880	225	36000
75	12000	400	16000
78	12480	410	17600
88	14080	420	19200
132	21120	425	20000
138	22080	431	20960
144	23040	437	21920
146	23360	440	22400
153	24480	447	23520
156	24960	450	24000
160	25600	455	24800
174	27840	470	27200
183	29280	482	29120
192	30720	495	31200
200	32000	520	35200
208	33280		

On selection of test mode, FM1300 radios tune to Channel 1. Low, mid and high alignment channel frequencies are stored in EEPROM and reference to the Equipment Data Sheet should be made to identify these.

KEYPAD CONSOLES (FM1200 only)

Receiver and Transmitter Frequencies

By "dialling-in" certain number strings via the Keypad Console it is possible to alter the transmitter and receiver codes.

Overwrite Tx Test Base Code:

Enter "202nnnnn #" where "nnnnn" is the new Tx Test Base Code number.

For Example;

to change the base code to 192MHz (code 30720), type "20230720" followed by "#".

Overwrite Rx Test Base Code:

Enter "201nnnnn #" where "nnnnn" is the new Rx Test Base Code number.

The radio will only respond to new base codes if a valid receiver base code is entered. If a transmitter base code only is entered, the radio will ignore this code and use the existing code. This does not preclude entering the existing receiver base code with a new transmitter code.

FFSK Signalling

The dialled strings used to control the FFSK encoder can be dialled directly from the console keypad, as follows:-

Enter "30000001#"	to transmit a 1200Hz tone.
Enter "30000002#"	to transmit a 1800Hz tone.
Enter "30000003#"	to encode 101.. sequence.
Enter "30000000#"	to disable tone output.

TEST DATA (FM1200 only)

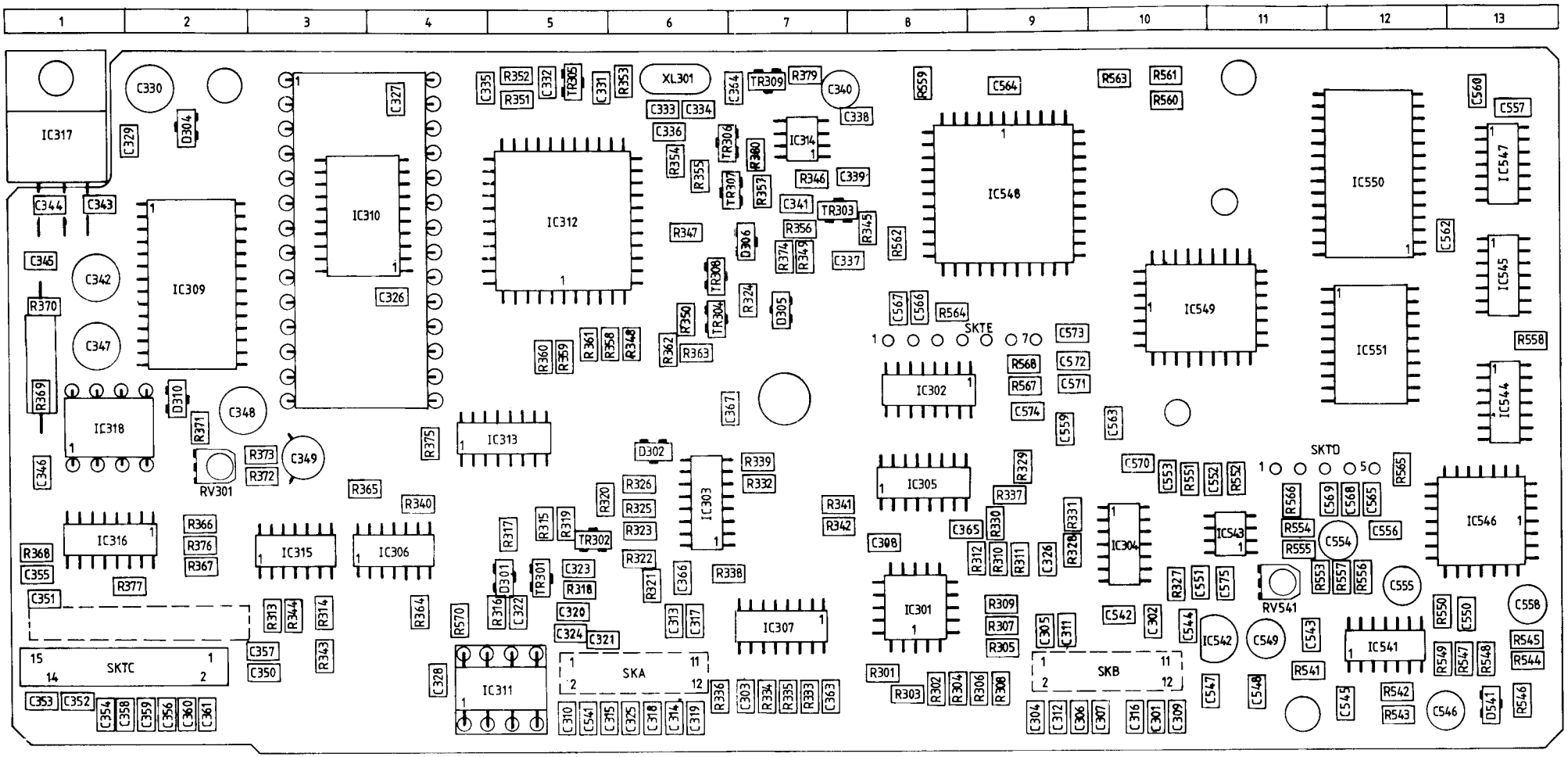
Calculation of Tx & Rx Synthesiser base codes

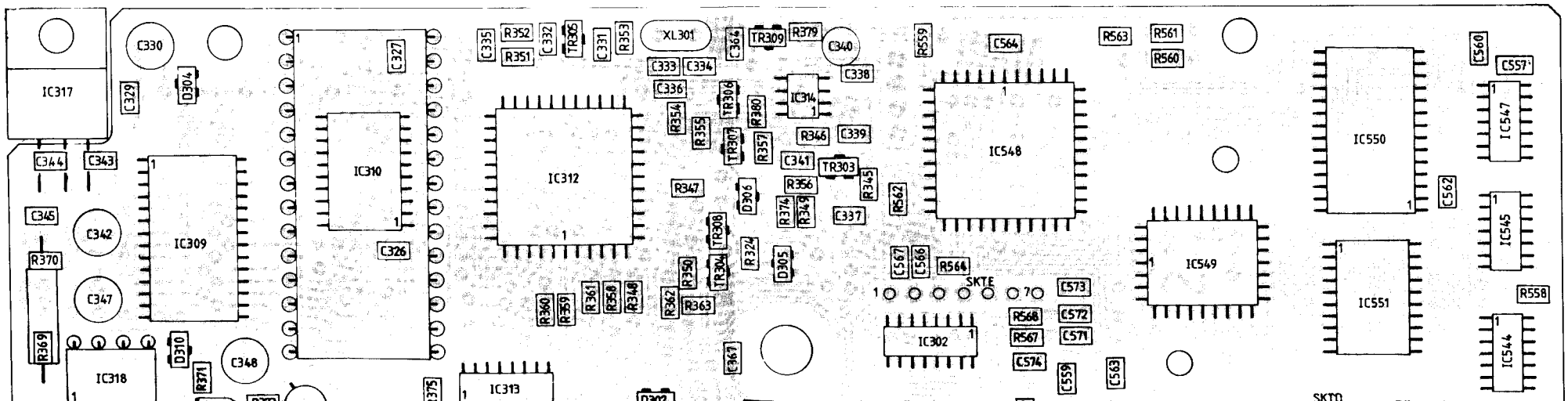
$$\text{Synthesiser Base Code} = \frac{\text{Channel Frequency - Base Frequency}}{\text{Reference Frequency}}$$

where:- Base Frequency = 0MHz for VHF and 300MHz for UHF Bands.

Reference Frequency

6,25kHz or 5,0kHz (depending on channel spacing)


1 2 3 4 5 6 7 8 9 10 11 12 13
A B C D E F
IC317
IC310
IC309
IC312
XL301
IC314
IC548
IC550
IC547
IC545
IC549
IC551
IC544
IC318
IC313
IC302
IC303
IC305
IC304
IC543
IC546
IC316
IC315
IC306
IC307
IC301
IC542
IC541
IC311
RV301
RV541
SKTC
SKA
SKB
SKTE
SKTD


IC317
IC310
IC309
IC312
XL301
IC314
IC548
IC550
IC547
IC545
IC549
IC551
IC544
IC318
IC313
IC302
SKTE
SKTD

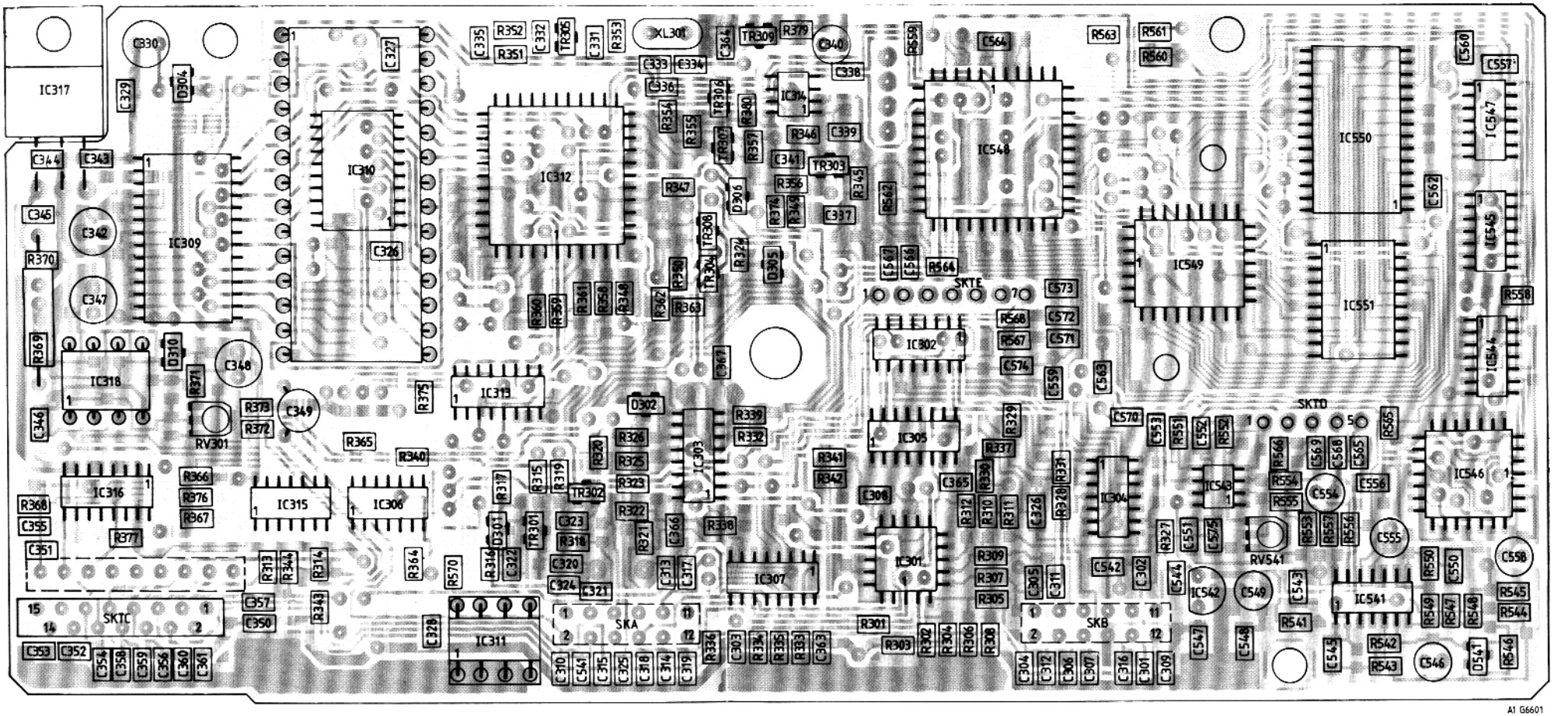


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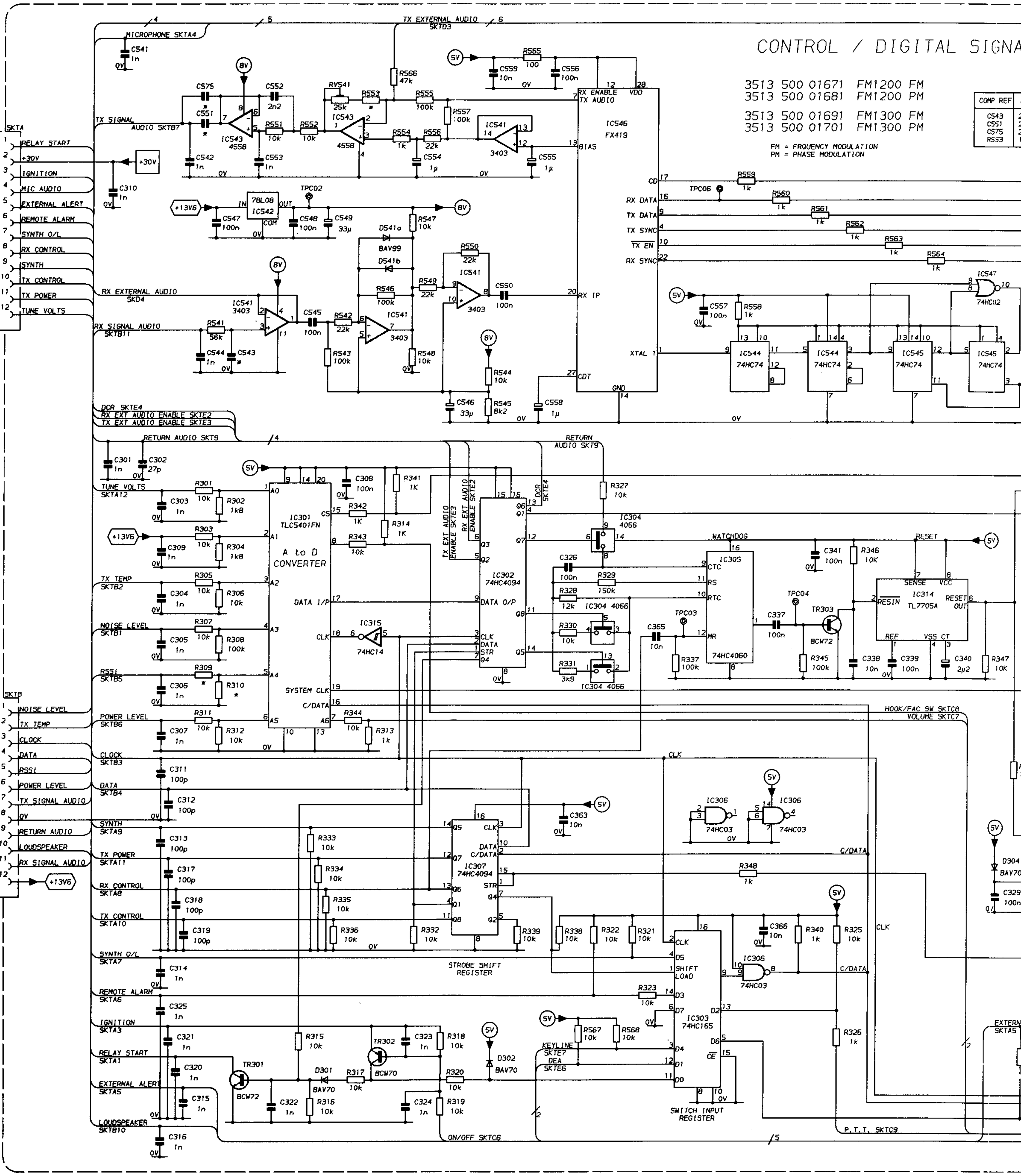
FIG 6.1 CONTROL/DIGITAL SIGNALLING PWB COMPONENT LOCATION DIAGRAM

CONTROL / DIGITAL SIGNA

3513 500 01671 FM1200 FM
3513 500 01681 FM1200 PM
3513 500 01691 FM1300 FM
3513 500 01701 FM1300 PM

FM = FREQUENCY MODULATION
PM = PHASE MODULATION



CONTROL / DIGITAL SIGNALLING ASSEMBLY

3513 500 01671 FM1200 FM
3513 500 01681 FM1200 PM

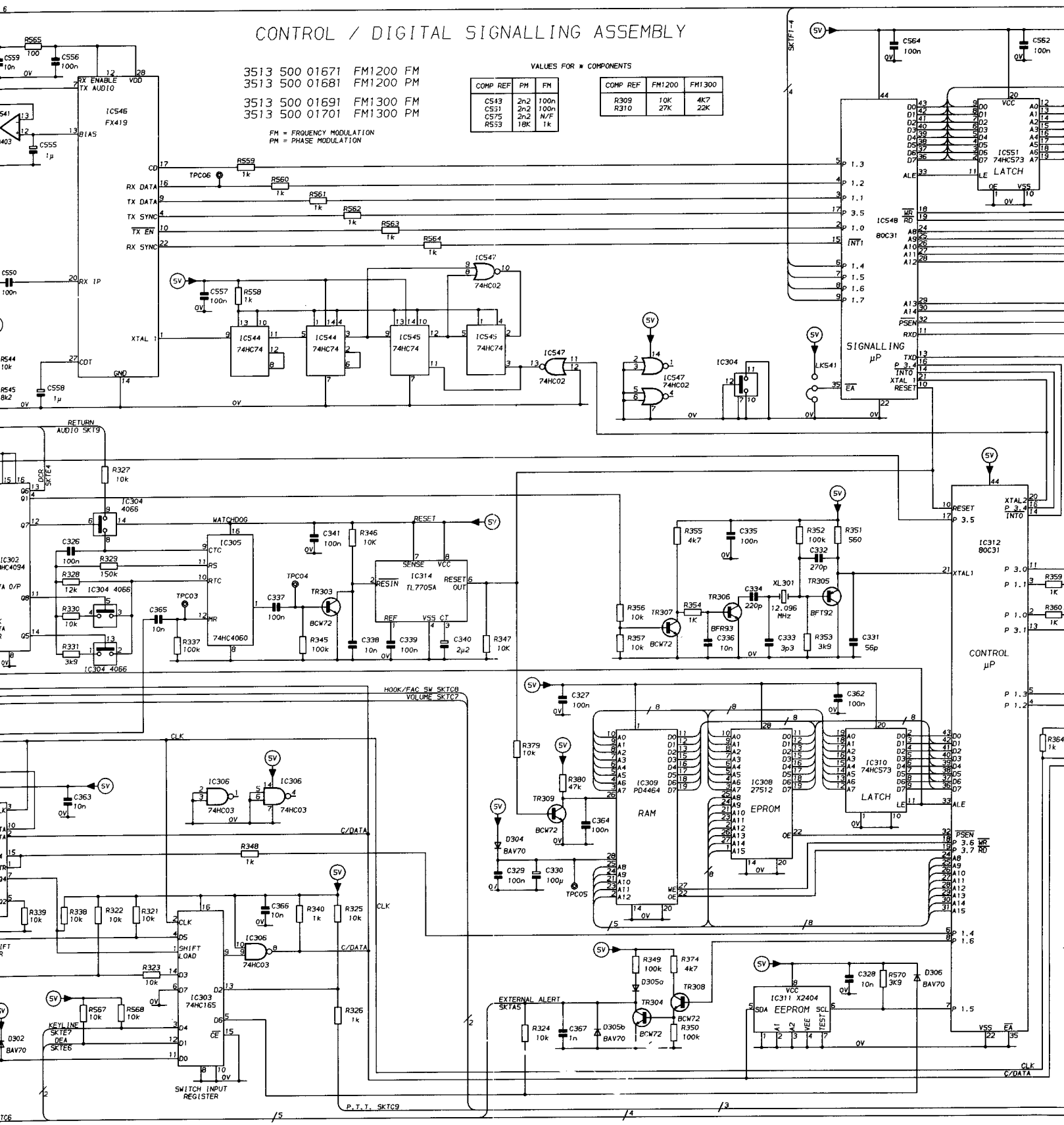
3513 500 01691 FM1300 FM
3513 500 01701 FM1300 PM

FM = FRQUENCY MODULATION
PM = PHASE MODULATION

VALUES FOR * COMPONENTS

COMP REF	PM	FM
C543	2n2	100n
C531	2n2	100n
C575	2n2	N/F
R533	18K	1k

COMP REF	FM1200	FM1300
R309	10K	4K7
R310	27K	22K



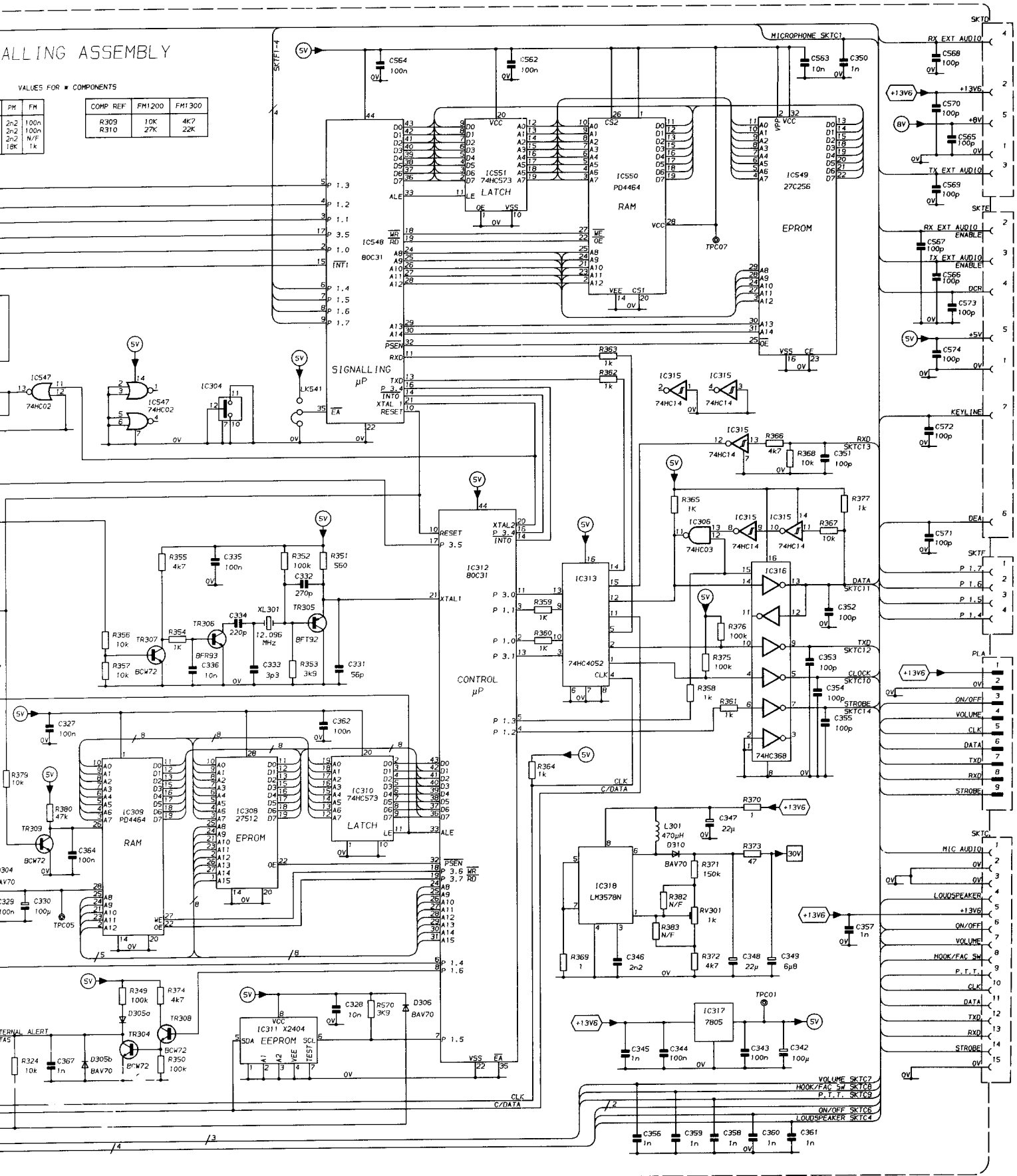


FIG 6.2 CONTROL/DIGITAL SIGNALLING PWB CIRCUIT DIAGRAM

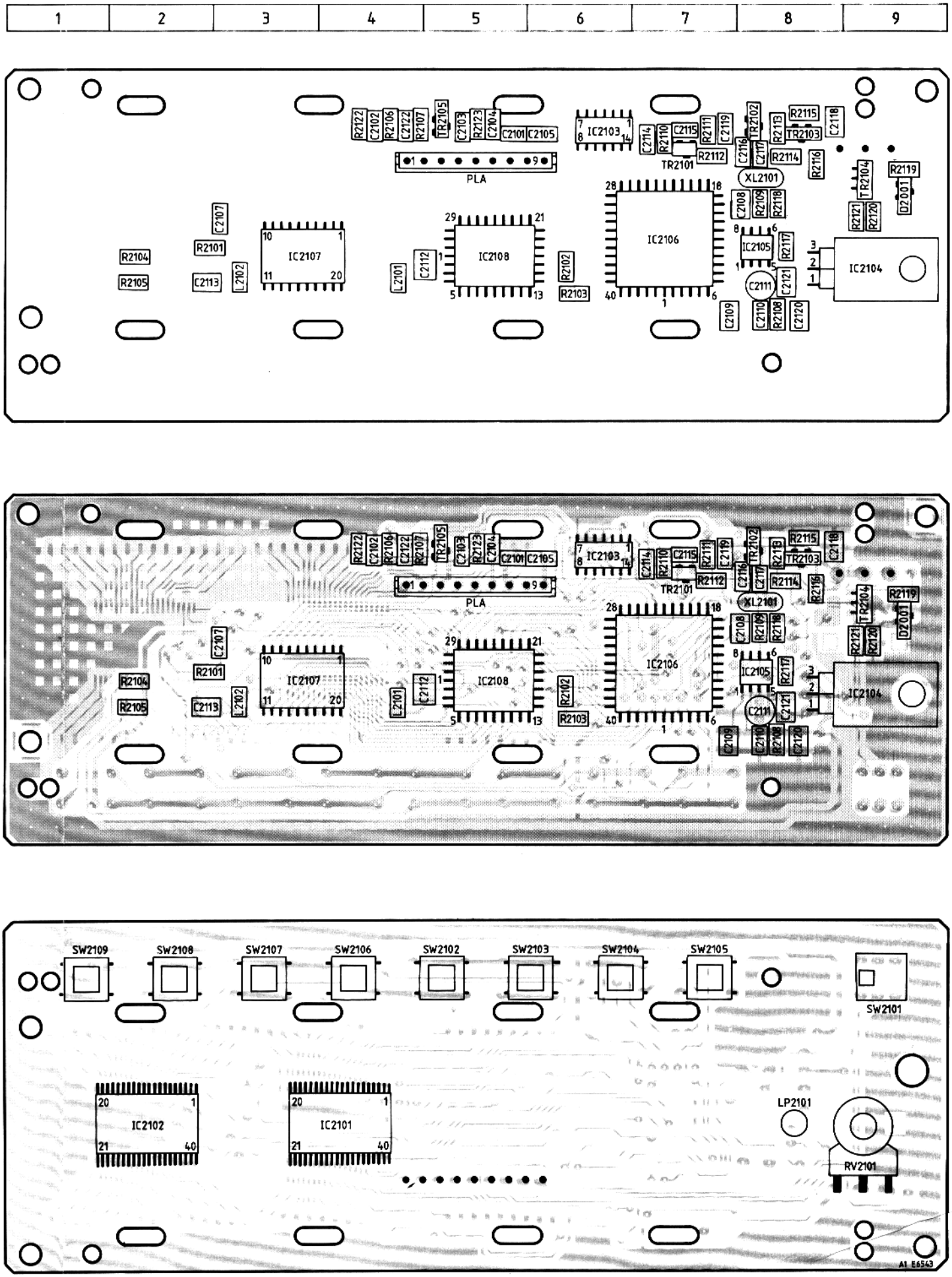
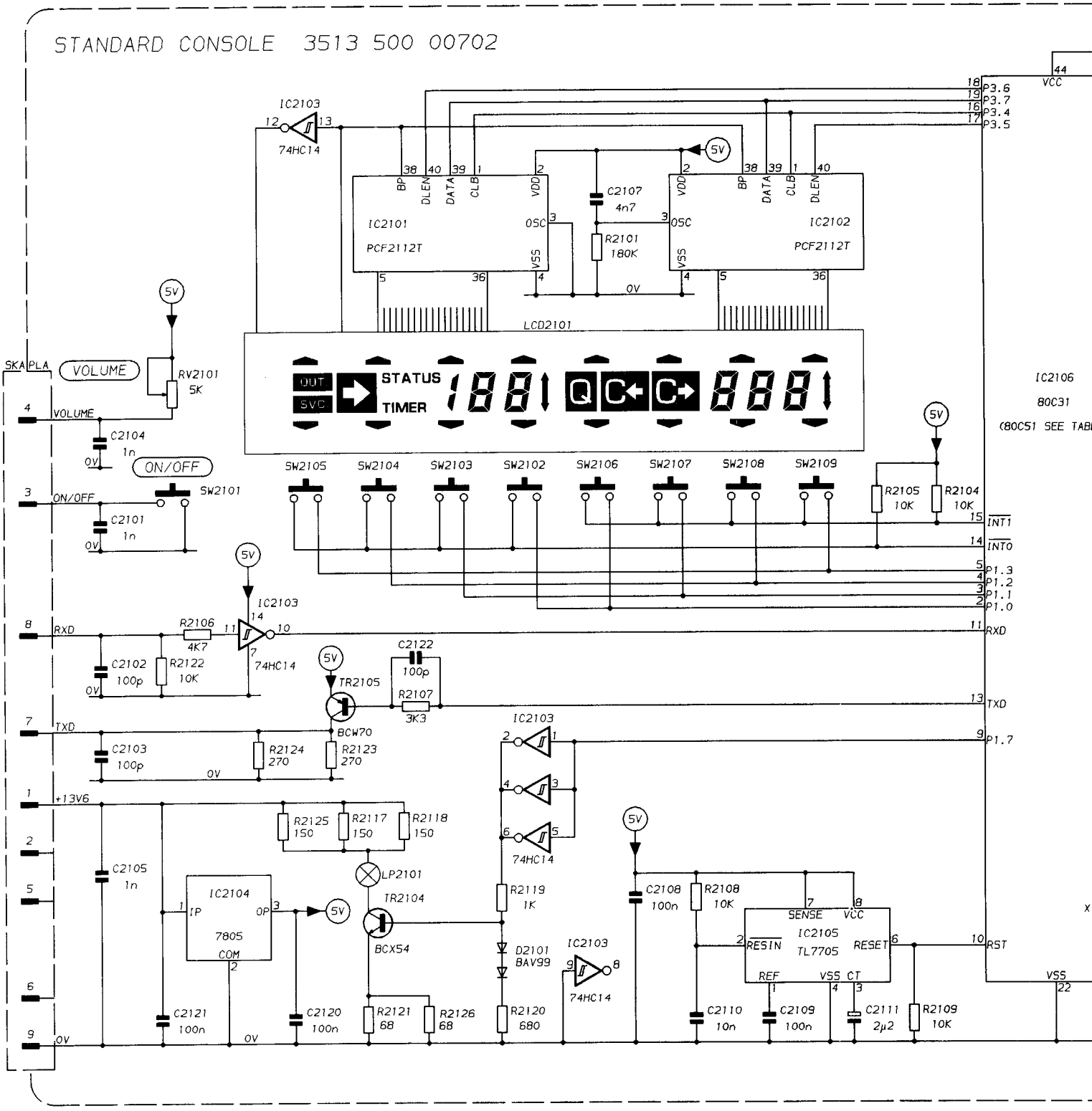


FIG 6.5 FM1200/FM1300 STANDARD CONSOLE COMPONENT LOCATION DIAGRAM

TP253A



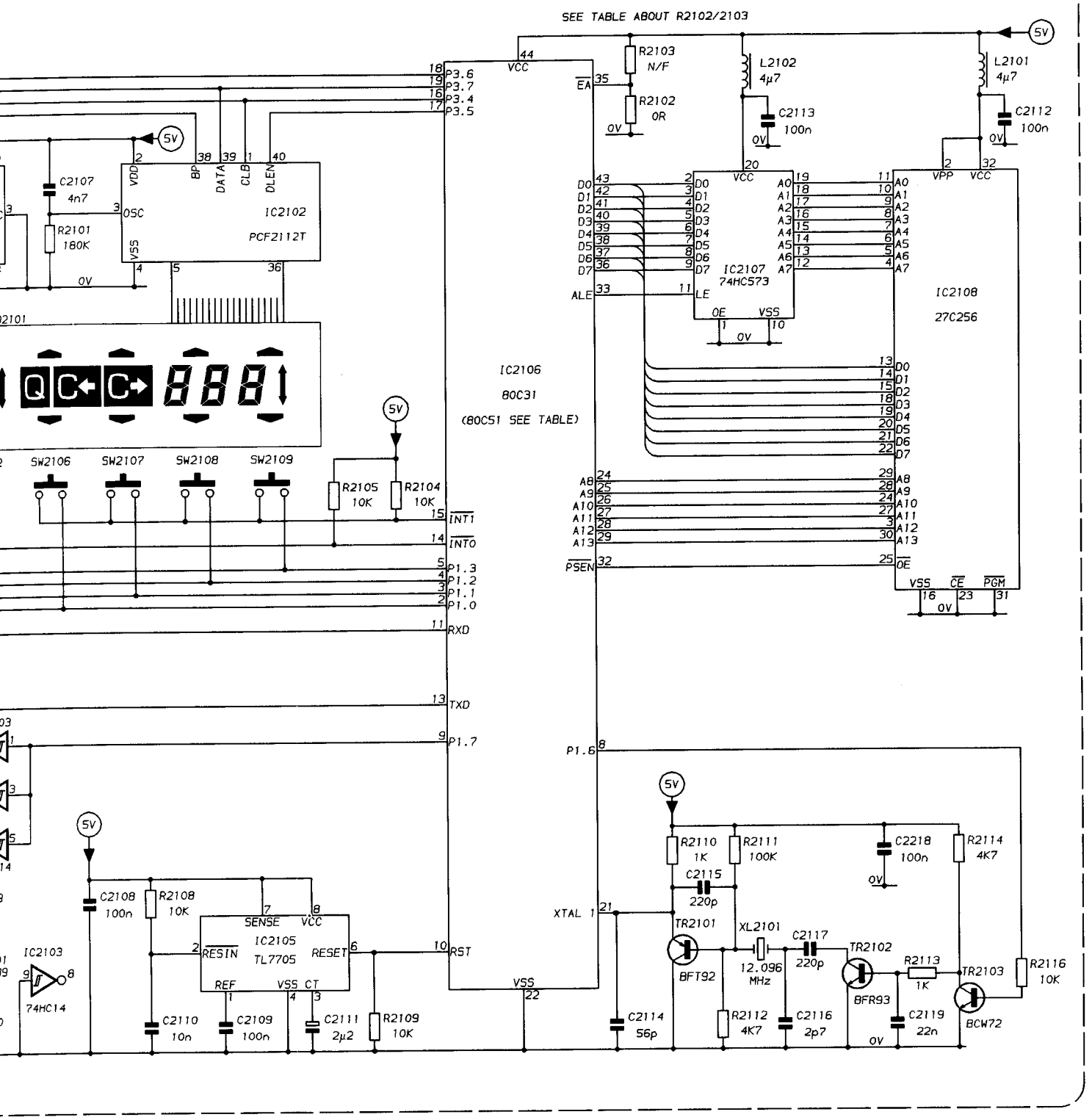
MEMORY ACCESS

IC2106 µP	MEMORY ACCESSED	IC2106 PIN 35	R2102	R2103	IC2107/2108
80C31	EXTERNAL	0V	FITTED	N/F	REQUIRED
80C51	EXTERNAL	0V	FITTED	N/F	REQUIRED
80C51	INTERNAL (MASKED)	5V	N/F	FITTED	NOT REQUIRED (MAY BE FITTED)

NOTES

1. N/F = NOT FITTED

FIG 6.6 FM1200/FM1300 STANDARD CONSOLE CIRCUIT DIAGRAM



MEMORY ACCESS

IC2106 µP	MEMORY ACCESSED	IC2106 PIN 35	R2102	R2103	IC2107/2108
80C31	EXTERNAL	0V	FITTED	N/F	REQUIRED
80C51	EXTERNAL	0V	FITTED	N/F	REQUIRED
80C51	INTERNAL (MASKED)	5V	N/F	FITTED	NOT REQUIRED (MAY BE FITTED)

0 STANDARD CONSOLE
RAM